Exhibit B

United States Patent and Trademark Office's June 17, 2016, Non-Final Rejection of Application No. 14/698,542

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/698,542	04/28/2015	Jong-Man IM	P14H0231/US	4396

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EXAMINER
COLE, BRANDON S

ART UNIT	PAPER NUMBER
2842	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/698,542	Applicant(s) IM ET AL.	
	Examiner BRANDON S. COLE	Art Unit 2842	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Aprill 28th 2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1 - 20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1 - 11 and 16 - 20* is/are rejected.

8)☒ Claim(s) *12 - 15* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *Aprill 28th 2016* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *4/28/215*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities:

Claim 2, lines 1 and 2, "control section" should be changed to -- control block --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

3. Claims 1 – 11 and 16 – 20 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by anticipated KOO et al (US 2015/0177763).

The applied reference has a common assignee with the instant application. Based upon the earlier effectively filed date of the reference, it constitutes prior art under 35 U.S.C. 102(a)(2). This rejection under 35 U.S.C. 102(a)(2) might be overcome by: (1) a showing under 37 CFR 1.130(a) that the subject matter disclosed in the reference was obtained directly or indirectly from the inventor or a joint inventor of this application and is thus not prior art in accordance with 35 U.S.C. 102(b)(2)(A); (2) a showing under 37 CFR 1.130(b) of a prior public disclosure under 35 U.S.C. 102(b)(2)(B) if the same invention is not being claimed; or (3) a statement pursuant to

35 U.S.C.102(b)(2)(C) establishing that, not later than the effective filing date of the claimed invention, the subject matter disclosed and the claimed invention were either owned by the same person or subject to an obligation of assignment to the same person or subject to a joint research agreement.

As to claim 1, KOO et al figures 1 – 3 that a semiconductor device comprising:

an internal voltage generation block (3) suitable for generating an internal voltage (INT) based on first (VDD2) and second (VDD1) external voltages whose power-up sections are different from each other; and

a control block (2) suitable for fixing the internal voltage to a predetermined voltage level during a control section including a first power-up section (22) of the first external voltage and a second power-up section (21) of the second external voltage.

As to claim 2, KOO et al figures 1 – 3 that the semiconductor device comprising, wherein the control section (2) includes an intermission (23) between the first (22) and second (21) power- up sections.

As to claim 3, KOO et al figures 1 – 3 that the semiconductor device, wherein a first power-up moment when the first power-up section (22) starts is earlier than a second power-up moment when the second power-up section (21) starts (Taught in paragraph [0020]).

As to claim 4, KOO et al figures 1 – 3 that the semiconductor device, wherein the control block (2) includes:

a detection unit (22, 21) suitable for detecting the first power-up section (22) based on the first external voltage (VDD2) and the second power-up section (21) based on the second external voltage (VDD1); and a driving unit (23) suitable for driving an internal voltage node to a ground voltage during the first and second power-up sections based on a detection result of the detection unit.

As to claim 5, KOO et al figures 1 – 3 that the semiconductor device, further comprising:

an internal circuit block (12) suitable for blocking a portion of an internal current path during the control section based on the internal voltage (INT).

As to claim 6, KOO et al figures 1 – 3 that the semiconductor device, wherein the internal voltage generation block (3) is disabled during the second power-up section (21) or the control section (2) based on the detection result of the detection unit (22, 21).

As to claim 7, KOO et al figures 1 – 3 that the semiconductor device,

a reference voltage generation block (31, 33) suitable for generating a reference voltage (nd32) corresponding to a seed voltage based on a second external voltage (VDD1);

an internal voltage generation block (32) suitable for generating an internal voltage (INT) to the reference voltage based on the first external voltage (VDD2), wherein the internal voltage generation block is disabled (CNT to block N31) in response to first (22) and/or second (21) power-up signals;

a detection block (22, 21) suitable for detecting a first power-up section (22) based on the first external voltage (VDD2) and a second power-up section (21) based on the second external voltage (VDD1) to output the first (PWRUP2) and second (PWRUP1)power-up signals; and

a driving block (23) suitable for driving an internal voltage node to a ground voltage during a control section including the first and second power-up sections in response to the first and second power-up signals.

As to claim 8, KOO et al figures 1 – 3 that the semiconductor device, wherein a first power-up moment, when the first power-up section (22) starts, is earlier than a second power-up moment when the second power-up section starts (21) (Taught in paragraph [0020]).

As to claim 9, KOO et al figures 1 – 3 that the semiconductor device, further comprising: a control block (2) suitable for fixing the reference voltage (nd32) to the ground voltage (VSS) during the second power-up section (21) or the control section in response to at least one of the first (PWRUP2) and second power-up signals (PWRUP1).

As to claim 10, KOO et al figures 1 – 3 that the semiconductor device, wherein the detection block (22, 21) includes:

a first detection circuit (22) suitable for detecting the first power-up section of the first external voltage (VDD2) to generate the first power-up signal (PWRUP2); and

a second detection circuit (21) suitable for detecting the second power-up section of the second external voltage (VDD1) to generate the second power-up signal (PWRUP1).

As to claim 11, KOO et al figures 1 – 3 that the semiconductor device, wherein the driving block (23) includes:

a first driving circuit (IV22) suitable for driving the internal voltage (INT) node to the ground voltage (VSS) during the first power-up section in response to the first power-up signal (PWRUP2); and

a second driving circuit (IV21) suitable for driving the internal voltage (INT) node to the ground voltage (VSS) during the second power-up section in response to the second power-up signal (PWRUP1).

Claim 16 has similar limitations as claim 7. Therefore, the claim is rejected for the same reasons as above.

Claim 17 has similar limitations as claim 7. Therefore, the claim is rejected for the same reasons as above.

Claim 18 has similar limitations as claim 8. Therefore, the claim is rejected for the same reasons as above.

Claim 19 has similar limitations as claim 8. Therefore, the claim is rejected for the same reasons as above.

As to claim 20, KOO et al figures 1 – 3 the method, wherein the internal current path (INT) includes a direct current path that is formed between a supply terminal of the second external voltage (VDD1) and a supply terminal of the ground voltage (VSS).

Allowable Subject Matter

4. Claims12 – 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is

(571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BRANDON S COLE/
Primary Examiner, Art Unit 2842